region **323** is biased in the forward direction. Here, if the minus voltage equal to or less than a breakdown voltage of the diode formed by the P^- base region **314** and the N^- collector region **313** is applied to the pad, the current flows from the power supply voltage (e.g. ground (GND) voltage) to the pad via the resistor R**12***i* and the resistor R**11***i*. Therefore, the voltage of the base terminal B**11***i* is increased due to a voltage drop by the current control resistor R**11***i*, and the transistor on the side of the pad is operated so that the surge current starts flowing from the power supply voltage (e.g. ground (GND) voltage) to the pad.

[0134] As described above, the surge current (or ESD current) flows via the transistor on the side of the power supply voltage (e.g. ground (GND) voltage) and the plurality of current control resistors R**12***i*, whereby current concentration in the transistor in the ESD protection element can be avoided. This effect is similarly observed in the transistor on the pad side. Even if a plus or minus large amplitude voltage is applied thereto, the large amplitude voltage is not applied to the transistors in the ESD protection element of the present embodiment, so that it is possible to avoid element destruction.

[0135] FIG. **27** is a plan view showing structure of a modification example of the ESD protection element according to the third embodiment of this invention. Referring to FIG. **27**, a modification example of the ESD protection element in the third embodiment will be described. Although the P^+ diffusion layers **16** are separately provided in the base width W direction (i.e. in the Y-axis direction) in the ESD protection element of the third embodiment, the P^+ diffusion layers **16** are connected to each other by the P^+ base diffusion layer **76** in the ESD protection element shown in FIG. **27**. The other structure is same as the third embodiment.

[0136] In detail, the P^+ base diffusion layers **16** in this example have a portion with a width L**3** in which the P^+ base diffusion layers **16** are partially separated by the element separation region **208** and a portion with a width L**2** in which the P^+ base diffusion layers **16** are continuously connected to each other in the based width direction by the P^+ base diffusion layer **76**. Here, the widths L**2** and L**3** are the widths in the direction perpendicular to the base width direction (i.e. in the X-axis direction). The width L**2** is desirable to be smaller than the width L**1** of the P^+ base diffusion layer **16** in the X-axis direction. Also, the width L**3** is desirable to be set to the size to an extent that the concentration of the surge current can be avoided. Therefore, the width L**3** is desirable to be larger than the width L**2**.

[0137] FIG. **28** is a plan view showing the structure of a modification example of the ESD protection element shown in FIG. **27**. FIG. **29** is a cross sectional view of the ESD protection element along I-I' section shown in FIG. **28**. Referring to FIGS. **28** and **29**, the modification example of the ESD protection element shown in FIG. **27** will be described. In the ESD protection element shown in FIG. **27**, the N^+ emitter diffusion layers **17** and the P^+ base diffusion layers **16** are separated by the element separation region **208** into the X-axis direction. However, in the ESD protection element shown in FIG. **28**, the N^+ emitter diffusion layers **17** and the P^+ base diffusion layers **16** are in contact with each other. That is, in the ESD protection element of this example, the element separation region **208** between the N^+ emitter diffusion layers **17** and the P^+ base diffusion layer **16** in the X-axis direction is removed, and both shows a batting structure which both are connected by a heterojunction.

[0138] When noise is received by the collector, a current due to the noise flows into junction capacitance (Ccb) and then flows to the power supply voltage (e.g. ground (GND) voltage) through the base. At this time, the noise current flows through base resistance Rbi to generate a voltage drop such that the voltage of the base B**2***i* (the base voltage) varies. In this case, the variation in the voltage of the base B**2***i* is (noise current)×Rbi; which becomes larger as the base resistance Rbi becomes larger. Also, the time period during which the change in the voltage of the base B**2***i* (the base voltage) at this time continues is determined based on Rbi×Ccb. If a diode composed of the emitter and the base is not turned on, any current does not flow through the emitter. However, when a time period during which the base voltage is higher than the emitter voltage because of the noise is equal to or longer than a time period required for the bipolar transistor to operate, the bipolar transistor becomes a conductive state. In order to avoid the bipolar operation due to the noise, a distance between the N^+ emitter diffusion layer **17** and the P^+ base diffusion layer **16** in this example is made shorter than that of the third embodiment, so that a current path between the N^+ emitter diffusion layer **17** and the P^+ base diffusion layer **16** through the P^- base region **204** is made short, resulting in that the resistance Rbi of the P^- base region **204** become small. As a result, (noise current)×Rbi and Rbi×Ccb become small and the start of the bipolar operation due to the noise is restrained.

[0139] In this way, by shortening the distance between the N^+ emitter diffusion layer **17** and the P^+ base diffusion layer **16**, a risk that the bipolar transistor operates due to the noise can be reduced. It should be noted that it is not always necessary to join the N^+ emitter diffusion layer **17** and the P^+ base diffusion layer **16** for such an effect. For example, in the third embodiment, the similar effect can be attained by shortening the width of the element separation region **208** between the emitter and the base.

[0140] FIG. **30** is a plan view showing the structure of the other modification example in the third embodiment. Referring to FIG. **30**, another modification example of the third embodiment will be described. In the ESD protection element of the third embodiment, a plurality of metal wirings **15** separated from each other in the base width W direction (i.e. in the Y-axis direction) are connected by a metal wiring **75** on the N^+ emitter diffusion layer **17**. The other structure is same as that of the third embodiment.

[0141] In the ESD protection element shown in FIG. **30**, the metal wiring **75** which connects the metal wirings **15** in the Y-axis direction on the emitter functions as a thermal capacitance to absorb heat generated by the ESD pulse current, whereby to attain the effect that the ESD protection performance is improved.

[0142] Although the various embodiments of the present invention have been described, specific structures are not limited to the above examples, and any modifications without going beyond the gist of the present invention are included within the present invention. The first to ninth embodiments can be combined in a range of no technical contradiction. For example, the base diffusion layer and the emitter diffusion layer in the first embodiment may be separated in the same manner as the third embodiment. The power supply voltage may be set to a different voltage other than the ground voltage. The present invention can be further applicable to an ESD protection element using a lateral PNP bipolar transistor and a lateral NPN bipolar transistor.